

WHAT IS CLAIMED IS:

1. An integrator circuit comprising:
 2. (a) an input conductor for conducting an input current;
 3. (b) an amplifier stage having an input coupled to the input conductor;
 4. (c) an integrating capacitor coupled between the input of the amplifier stage and an output of the amplifier stage; and
 5. (e) an MOS capacitor coupled between an output of the amplifier stage and a voltage conductor for biasing the MOS capacitor.

1. 2. An integrator circuit comprising:
 2. (a) an input conductor for conducting an input current;
 3. (b) a first amplifier stage having an input coupled to the input conductor ;

4 (c) a second amplifier stage having an output and also having an input
5 coupled to an output of the first amplifier stage;

6 (d) an integrating capacitor coupled between the input of the first amplifier
7 stage and the output of the second amplifier stage; and

1 3. The integrator circuit of claim 2 wherein the first amplifier stage includes an input
2 stage having an output coupled to an input of a folded cascode stage, an output of the folded
3 cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the
4 MOS capacitor being coupled to the output of the second amplifier stage.

1 4. The integrator circuit of claim 3 wherein the first and second amplifier stages co-
2 act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its
3 accumulation region for low values of the input current to provide a high value of compensation
4 capacitance for the integrator circuit and so as to bias the MOS capacitor in its inversion region

5 for high values of the input current to provide a low value of compensation capacitance for the
6 integrator circuit.

1 5. The integrator circuit of claim 4 wherein the input current is a photodiode current
2 containing a relatively low amount of noise for the low values of the input current and containing
3 a higher amount of noise for the high values of the input current, and wherein an amount of noise
4 produced by the integrator circuit when the value of the compensation capacitance is high is
5 masked by the relatively high amount of noise.

1 6. The integrator circuit of claim 2 wherein the first amplifier stage is a non-
2 inverting amplifier stage and the second amplifier stage is an inverting amplifier stage.

1 7. The integrator circuit of claim 2 wherein the MOS compensation capacitor
2 includes an N-channel source region and an N-channel drain region both coupled to the input of
3 the second stage amplifier, and also includes a gate disposed over a channel region between the
4 N-channel source region and the N-channel drain region, the gate being coupled to the output of

5 the second amplifier stage.

1 8. The integrator circuit of claim 7 wherein the integrating capacitor is a poly
2 capacitor.

1 9. The integrator circuit of claim 2 wherein the input of the first amplifier stage
2 conducts a single-ended input signal.

1 10. The integrator circuit of claim 2 wherein the input of the first amplifier stage
2 conducts a differential input signal.

1 11. The integrator circuit of claim 6 wherein the second stage amplifier is an inverting
2 class A amplifier.

1 12. A CT scanner data acquisition system comprising:

2 (a) a plurality of integrator circuits, each including

3 i. an input conductor for conducting an input current,

4 ii. a first amplifier stage having an input coupled to the input

5 conductor,

6 iii. a second amplifier stage having an output and also having an input

7 coupled to an output of the first amplifier stage,

8 iv. an integrating capacitor coupled between the input of the first

9 amplifier stage and the output of the second amplifier stage, and

10 v. an MOS compensation capacitor coupled between the input and

11 output of the second amplifier stage;

12 (b) a plurality of photodiodes each having an anode coupled to an input

13 conductor of an integrator circuit, respectively;

14 (c) a plurality of analog-to-digital converters, inputs of the analog-to-digital

15 converters being coupled to the outputs of various integrator circuits.

1 13. The CT scanner data acquisition system of claim 12 wherein the first amplifier
2 stage includes an input stage having an output coupled to an input of a folded cascode stage, an
3 output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a
4 second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

1 14. The CT scanner data acquisition system of claim 13 wherein the second amplifier
2 stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor
3 in its accumulation region for low values of the input current to provide a high value of
4 compensation capacitance for the integrator circuit and so as to bias the MOS capacitor in its
5 inversion region for high values of the input current to provide a low value of compensation
6 capacitance for the integrator circuit.

1 15. The integrator circuit of claim 14 wherein the input current is a photodiode
2 current containing a relatively low amount of noise for the low values of the input current and
3 containing a relatively high amount of noise for the high values of the input current, wherein an
4 amount of noise produced by the integrator circuit when the value of the compensation
5 capacitance is high is masked by the relatively high amount of noise.

1 16. The CT scanner data acquisition system of claim 12 wherein the analog-to-digital
2 converters are delta-sigma analog-to-digital converters.

1 17. The CT scanner data acquisition system of claim 12 wherein the inputs of the
2 analog-to-digital converters are coupled to common outputs of groups of the integrator circuits,
3 respectively.

1 18. The CT scanner data acquisition system of claim 12 wherein the first amplifier
2 stage is an operational amplifier stage and the second amplifier stage is an inverting amplifier
3 stage.

1 19. The CT scanner data acquisition system of claim 12 wherein the MOS
2 compensation capacitor includes an N-channel source region and an N-channel drain region both
3 coupled to the input of the second stage amplifier, and also includes a gate disposed over a
4 channel region between the N-channel source region and the N-channel drain region, the gate
5 being coupled to the output of the second amplifier stage.

1 20. The CT scanner data acquisition system of claim of 19 wherein the integrating
2 capacitor is a poly capacitor.

1 21. The CT scanner data acquisition system of claim 12 wherein the input of the first
2 amplifier stage conducts a single-ended input signal.

1 22. The CT scanner data acquisition system of claim 12 wherein the input of the first
2 amplifier stage conducts a differential input signal.

1 23. The CT scanner data acquisition system of claim 12 wherein the second stage
2 amplifier is an inverting class A amplifier.

1 24. A method of operating an integrator circuit comprising:

2 (a) conducting an input current into an input of an amplifier stage;
3 (b) charging an integrating capacitor coupled between the input and an output
4 of the amplifier stage in response to the input current; and
5 (c) compensating the integrator circuit by controlling the bandwidth of the
6 integrator circuit by biasing an MOS capacitor coupled to the output into a predetermined
7 operating region range.

1 25. A method of operating an integrator circuit, comprising:

2 (a) conducting an input current into an input conductor of a first amplifier

3 stage;

4 (b) coupling an input of a second amplifier stage to an output of the first
5 amplifier stage;

6 (c) charging an integrating capacitor coupled between the input of the first
7 amplifier stage and an output of the second amplifier stage; and

8 (e) compensating the integrator circuit by controlling the bandwidth of the
9 integrator circuit by biasing an MOS compensation capacitor coupled between the input and
10 output of the second amplifier stage into a predetermined operating region range.

1 26. A method of operating a CT scanner data acquisition system, comprising:

2 (a) in each of a plurality of integrator circuits,

3 i. conducting an input current into an input conductor of a first
4 amplifier stage,

5 ii. coupling an input of a second amplifier stage to an output of the

- 6 first amplifier stage,
- 7 iii. charging an integrating capacitor coupled between the input of the
- 8 first amplifier stage and an output of the second amplifier stage; and
- 9 iv. compensating the integrator circuit by controlling the bandwidth of
- 10 the integrator circuit by biasing an MOS compensation capacitor coupled between the input and
- 11 output of the second amplifier stage into a predetermined operating region range;
- 12 (b) coupling an anode of each of a plurality of photodiodes to an input
- 13 conductor of a group of integrator circuits, respectively;
- 14 (c) coupling inputs of a plurality of analog-to-digital converters to the outputs
- 15 of various groups of integrator circuits, respectively.